CLAIMS

What is claimed is:

1. A monolithic array amplifier comprising:

a plurality of amplification units arranged in a grid-like structure on a monolithic substrate; and

a grid-bias network separating the amplification units to provide DC power to the amplification units,

wherein each amplification unit comprises bias-line bypass circuits in a periodic structure.

2. The array amplifier of claim 1 wherein each bias-line bypass circuit is positioned along bias streets of the grid-bias network and the bias-line bypass circuits are positioned at least partially around each amplification unit within a grid unit to reduce RF current flow between an associated one of the amplification units and the grid-bias network.

3. The array amplifier of claim 1 wherein each bias-line bypass circuit includes resistive-inductive-capacitance networks comprising:

thin-film capacitors;

inductive wire bridges coupling the capacitors to bias streets of the grid-bias network; and

thin-film resistors coupling the capacitors to ground vias.

4. The array amplifier of claim 3 wherein the capacitors of each bias line circuit have differing values selected to resonate with the inductive wire bridges and the thin-film resistors to shunt RF current flow over a range of RF frequencies.

5. The array amplifier of claim 3 further comprising second thin-film capacitors coupled between more than one ground vias with second thin-film

resistors, and further coupled with the grid-bias network with second inductive wire bridges.

6. The array amplifier of claim 3 wherein the inductive wire bridges comprise inductive wire-bridge fuses, the fuses to provide an open circuit when an associated one the thin-film capacitors shorts to ground.

7. The array amplifier of claim 1 wherein the monolithic substrate comprises a semiconductor material, and wherein the bias-line bypass circuits are positioned along a bias street of the grid-bias network and spaced apart by less than a quarter-wavelength of an effective propagation constant of the bias street, and

wherein the semiconductor material comprises a material selected from the group consisting of Indium-Phosphide (InP), Gallium Arsenide (GaAs), Gallium Nitride (GaN), and Silicon (Si).

8. The array amplifier of claim 1 wherein each amplification unit comprises a power amplifier which receives a bias voltage from the grid-bias network.

9. The array amplifier of claim 7 wherein the power amplifier comprises a self-biased high-electron-mobility transistor (HEMT) amplifier.

10. The array amplifier of claim 1 wherein at least some of the amplification units of the plurality comprise:

a receive antenna;

a transmit antenna; and

a power amplifier to receive a bias voltage from the grid-bias network and to amplify millimeter-wave frequencies received by the receive antenna for transmission by the transmit antenna.

11. The array amplifier of claim 10 wherein the receive antennas are configured to receive a substantially vertically-polarized wavefront at a

millimeter-wave frequency, the power amplifiers are configured to amplify signals to provide a substantially horizontally-polarized wavefront, and the transmit antennas are configured to transmit the amplified signals to generate the high-power collimated wavefront at the millimeter-wave frequency.

12. The array amplifier of claim 3 wherein the grid-bias network comprises a mesh structure comprising gold having a thickness of approximately between 20 and 30 microns and a width between approximately 200 and 400 microns,

wherein a power source provides up to 300 amps of current to the grid-bias network, and wherein the capacitors range between approximately 0.05pf and 10.0pf.

13. A method of decoupling a bias structure in a monolithic array amplifier comprising:

providing DC power to a plurality of amplification units arranged in a grid-like structure with a grid-bias network separating the amplification units; and

reducing RF current flow between the amplification units and the grid-bias network with a periodic structure of bias-line bypass circuits within each of the amplification units.

14. The method of claim 13 wherein reducing comprises shunting RF current flow over a range of RF frequencies with a plurality of RLC networks that comprise each bias-line bypass circuit, each bias-line bypass circuit comprising thin-film capacitors, inductive wire bridges coupling the capacitors to bias streets of the grid-bias network, and thin-film resistors coupling the capacitors to ground vias, wherein the capacitors of each bias line circuit have differing values selected to resonate with an associated one of the thin-film resistors and an associated one of the inductive wire bridges.

15. The method of claim 14 further comprising:

providing second thin-film capacitors between more than one of the ground vias, the second thin-film capacitors coupled to the more than one of the ground vias with second thin-film resistors; and

providing second inductive wire bridges coupling the second thin-film capacitors with the grid-bias network.

16. The method of claim 14 wherein the inductive wire bridges comprise inductive wire-bridge fuses, and the method further comprises providing an open circuit with the inductive wire-bridge fuses when an associated one the thin-film capacitors shorts to ground.

17. The method of claim 13 wherein the monolithic substrate comprises a semiconductor material, and wherein reducing comprises positioning the bias-line bypass circuits along a bias street of the grid-bias network to have a spacing of less than a quarter-wavelength of an effective propagation constant of the bias street.

18. The method of claim 13 wherein at least some amplification units of the plurality comprise a receive antenna, a transmit antenna, and a power amplifier.

19. The method of claim 18 further comprising:

providing each power amplifier with a bias voltage from the grid-bias network; and

amplifying millimeter wave signals received by the receive antenna for transmission by the transmit antenna.

20. A bias-line bypassing structure comprising a plurality of bias-line bypass circuits positioned in a periodic structure at least partially around each of a plurality of circuit elements to reduce RF current flow between the circuit elements and a grid-bias network for providing bias current to the circuit elements.

21. The structure of claim 20 wherein each bias-line bypass circuit comprises thin-film capacitors, inductive wire bridges coupling the capacitors to bias streets of the grid-bias network, and thin-film resistors coupling the capacitors to ground vias, wherein the capacitors have differing values selected to

resonate with an associated one of the inductive wire bridges and an associated one of the thin-film resistors to shunt RF current flow over a range of RF frequencies.

22. The structure of claim 21 wherein the inductive wire bridges comprise inductive wire-bridge fuses, the fuses to provide an open circuit when an associated one the thin-film capacitors shorts to ground.

23. The structure of claim 21 wherein the plurality of circuit elements are arranged in a grid-like structure and fabricated on a single monolithic substrate, the plurality of circuit elements and the bias-line bypass circuits being within grid units separated by bias streets which form the structure.

24. The structure of claim 22 wherein the grid-bias network is power-grid mesh separating the circuit elements for providing DC power to the circuit elements.

25. The structure of claim 20 wherein the bias-line bypass circuits further comprise second thin-film capacitors coupled between more than one ground vias with second thin-film resistors, and coupled with the grid-bias network with second inductive wire bridges.

26. The structure of claim 23 wherein the monolithic substrate comprises a semiconductor material, and wherein the bias-line bypass circuits are positioned along the bias streets of the grid-bias network and spaced apart by less than a quarter-wavelength of an effective propagation constant of the bias street.

27. The structure of claim 26 wherein the semiconductor material comprises a material selected from the group consisting of Indium-Phosphide (InP), Gallium Arsenide (GaAs), Gallium Nitride (GaN), and Silicon (Si).

27. The structure of claim 21 wherein each circuit element comprises a receive antenna, a transmit antenna, and a power amplifier to receive a bias

voltage from the grid-bias network and to amplify a millimeter wave signals received by the receive antenna for re-transmission by the transmit antenna.

28. The structure of claim 21 wherein the grid-bias network comprises a mesh structure comprised of gold having a thickness of approximately between 20 and 30 microns and a width between approximately 200 and 400 microns.

29. The structure of claim 28 wherein a power source provides up to 300 amps of current to the grid-bias network, and wherein the capacitors range between approximately 0.05pf and 10.0pf.